REMARKS

I. Status of Claims

Claims 1-13 and 16-22 are pending in the application. Claims 1, 6 and 11 are independent. Claims 1, 6, 17, and 22 are currently amended. Claims 14-15 are canceled without prejudice to and/or disclaimer of the subject matter therein.

Claims 1, 14, 16, 17 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Kinzer et al. (USP 6,194,741) ("Kinzer").

Claims 3-5, 9, 10 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Kinzer et al. in view of WO 99/52152 ("WO 99/52152").

Claims 6, 8, 15, 19-22 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Kinzer et al. in view of WO 99/52152.

The Applicant respectfully requests reconsideration of these rejections in view of the foregoing amendments and the following remarks.

II. Allowable Subject Matter

Claims 11-13 and 18 are allowed.

Claims 2 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

III. Pending Claims

Claims 1 and 6, the only independent claims currently rejected, stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Kinzer, and Kinzer in view of WO 99/52152, respectively.

The Applicant respectfully submits that claims 1 and 6 are patentable over the cited references at least because they recite, "...the space between the adjacent floating regions is a space where positive field intensity distribution curves connect with each other during the off time of the gate electrode voltage,..." and "...the deposited insulating layer having a thickness capable of forming peaks of a electric field at two positions in a direction of thickness of the

semiconductor substrate during the off time of the gate electrode voltage."

The Applicant respectfully submits that the inventions of claims 1 and 6 are distinguished from the cited references at least by the following two points.

The first feature that distinguishes the claims from the cited references is that a depleted layer expanding from a floating P layer becomes continuous with a depleted layer expanding from an adjacent floating P layer. Each depleted layer laterally expands so that the adjacent depleted layers connect with each other, forming an N drift layer, depleted from both sides to support/withstand voltage between drain and source. More specifically, the withstand voltage is supported at two positions; a PN junction of a P body region and an N drift layer and an PN junction of the floating P and the N drift layer. If the depleted layers of the adjacent floating P layers in the lateral direction are not continuous with each other, the withstand voltage between drain and source will be supported by only the PN Junction of the P body region and the N drift layer. The Applicant respectfully submits that Kinzer does not describe such a configuration.

Further, if the space between the floating P layers is too wide, a black portion in Fig. 23 where no electric field occurs can traverse vertically between the adjacent floating P layers. However, in the space of the inventions of claims 1 and 6, positive field intensity distribution curves connect with each other.

In contrast to the inventions of claims 1 and 6, Kinzer, such as in Fig. 6, shows that the bottom of a gate dielectric 34 is located around the middle of the floating P layer and the P body region. The distance between the floating P layer and the bottom line of the gate dielectric 34 is 1.0 p, and the distance between the P body region and the gate bottom line of the dielectric 34 can also be considered as equal. In this positional relationship, the depleted layer expanding from the PN junction of the P body region and the N drift layer and the depleted layer expanding from the PN junction of the floating P layer and the N drift layer will more than likely quickly connect with each other in a vertical direction. Only the upper depleted layer expanding from in the PN junction of the P body region and the N drift layer can serve to support withstand voltage.

The second feature of the inventions of claim 1 and 6 that distinguishes them from the cited references is that they are configured such that the depleted layer expanding from the PN junction of the P body region and the N drift layer can sufficiently support and/or withstand voltage. Further, the depleted layer can connect with the floating layer. The depleted layer

between the floating P layer and the N drift layer can also support withstand voltage between drain and source.

This second feature is first achieved by locating a lower end of a gate electrode above an upper end of a floating region so that a space between a lower surface of a body region and the upper end of the floating region is wider than a space between a lower end of a deposited insulating layer and a lower end of the floating region. Thus, a space between the lower end of the gate electrode and the lower end of the deposited insulating layer is wider than a space between the lower surface of the body region. Moreover, the upper end of the floating region and the thickness of the deposited insulated layer is a thickness enough to form peaks of electric field at two positions in a direction of thickness.

Consequently, it is possible to support electric fields of the PN Junction of the P body region and the N drift layer and the PN junction of the floating P layer and the N drift layer up to near a critical electric field, respectively. Thus, the withstand voltage between drain and source can be enhanced. If the thickness of the deposited insulating layer is too large, the upper and lower depleted layers will not connect with each other and therefore peaks of electric field will not be formed at two positions.

Furthermore, owing to small floating P layer, the floating P will not interrupt the flow of electric current during the ON time of gate voltage, the floating P will not connect quickly with the depletion layer expanding from the PN junction of the P body region and the N drift layer during the OFF time of gate voltage and will connect with the depletion layer after sufficiently supporting an electric field in the depletion layer expanding from the PN junction of the P body region and the N drift layer. Thus, withstand voltage can be supported at two positions (withhold voltage between drain and source can be supported at two positions while the peaks of electric field are increased up to near a critical electric field).

Still further, in Kinzer and WO99/52152, which utilize SiC, a diffusion layer is very difficult to form. In addition, the Applicant respectfully submits that it is also hard to come up with the formation of the diffusion layer in a circular shape by using SiC.

The Applicant respectfully submits that Kinzer does not disclose the above-identified configurations for withstanding voltage.

In addition, the Applicant respectfully submits that lacking any teaching and/or identifying reason why one of ordinary skill in the art would modify the cited references in the

manner as claimed by the Applicant, the references do not anticipate and/or render obvious the Applicant's invention. The Applicant respectfully submits that, as discussed in *KSR Int'l Co. v. Teleflex, et al.*, No. 04-1350, (U.S. Apr. 30, 2007), it remains necessary to identify the reason why a person of ordinary skill in the art would have been prompted to combine alleged prior art elements in the manner as claimed by the Applicant.

Therefore, the Applicant respectfully submits that, for at least these reasons, claims 1 and 6, as well as their dependent claims are patentable over the cited references.

IV. Paper and Award

We note that attached herewith in the Appendix is a paper illustrating the effects of using embodiments of the present invention to follow two peaks of a electrical field to support withstand voltage is effective. The paper published in an IEEE journal (and for which the Applicant's received an award—International Symposium on Power Semiconductor Devices & ICs 2005 Best Paper Award).

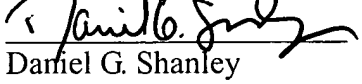
V. Conclusion

In light of the above discussion, the Applicant respectfully submits that the present application is in all aspects in allowable condition, and earnestly solicits favorable reconsideration and early issuance of a Notice of Allowance.

The Examiner is invited to contact the undersigned at (202) 220-4420 to discuss any matter concerning this application. The Office is authorized to charge any fees or credit any overpayment related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

Dated: August 22, 2008

By: 
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APPENDIX

Proceedings of the 17th International Symposium on Power Semiconductor Devices & IC's
May 23-26, 2005 Santa Barbara, CA

Floating Island and Thick Bottom Oxide Trench Gate MOSFET (FITMOS)

-A 60V Ultra Low On-Resistance Novel MOSFET with Superior Internal Body Diode-

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Abstract

A MOSFET structure named FITMOS has been successfully developed that exhibits record-low loss in the 60 volts breakdown voltage range. The breakdown voltage of 64 volts and specific on-resistance of 22mΩmm² (Vgs=15V) this performance exceeds the unipolar limit (1). The device has a body diode with superior reverse recovery characteristics and exhibits an extremely small value for RonQgd. The distinctive feature of this device is the use of floating islands formed by self-alignment and trench gates with a thick oxide layer on the bottoms. This structure can also be used for the terminal portion of the device, so the increase in the number of fabrication processes is less than 5%. Moreover, the rate of non-defective gates in 3-by-4-mm rectangular devices on an 8-inch wafer is at least 98%.

Introduction

The MOSFET is a key device for automobiles, with approximately 200 such devices used per vehicle. The role played by power electronics in automobiles is growing steadily (2-4), and there is no doubt that this makes the role of the MOSFET even more important. The automotive demand for DC-DC converters, inverters, and the like is growing, and MOSFETs are required not only to have low on-resistance, but also lower RonQgd, as well as a body diode with superior reverse recovery characteristics to suppress radio noise generation and voltage surges. An automotive MOSFET that satisfies these requirements has been developed that contributes to further progress in on-board electronic systems. The ratios of the resistance components that make up the on-resistance of the MOSFET are shown in Table 1. Fig. 1 shows the simulation model that was used for the calculations. The surface structure is the same, regardless of the breakdown voltage of the model, and the epitaxial concentration and epitaxial thickness were modified to create the optimum model for the calculations. With a low breakdown voltage of 30 volts, 84% of the on-resistance consists of channel resistance, so miniaturization would be an effective way to reduce the on-resistance. But with a breakdown voltage of 600 volts, 99% of the on-resistance is made up of drift resistance, so the best way to lower the on-resistance would be to reduce drift resistance by adopting a super junction structure, for example. The breakdown voltages used in automotive systems are in the intermediate range, from 60 to 100 volts, so both technologies, miniaturization and drift resistance reduction, are required. With a super junction structure, using a multi-epitaxial process (5) makes miniaturization difficult, and the trench-plus-epitaxial process (6) raises issues such as epitaxial crystallinity. It has also been noted that the recovery surge of the body diode in a super junction structure is high (7), so a new structure is required that can both improve the reverse recovery characteristics and reduce the drift resistance. The buried P layer (8) has been proposed as an alternative to the super junction structure, but it presents problems for miniaturization. It was in the context of all these considerations that a new MOSFET structure was developed that not only reduces channel resistance through miniaturization and reduces drift resistance by means of floating islands formed by self-alignment, but also has a body diode with superior recovery characteristics.

Table 1 On-resistance components

Breakdown voltage		30V	70V	600V
Resistance components	Channel	84%	22%	1%
	Drift	15%	78%	99%
	Other	1%	0%	0%

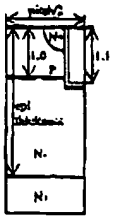


Fig. 1 Simulation model (units: μm)

Device Structure & Simulation

Fig. 2 shows the cross sectional structure of the new MOSFET that was developed. A diffusion layer is formed at the bottom of each trench, and the bottom portion of the trench is then buried by a thick oxide layer. The overall layout is shown in Fig. 3. It consists of a striated transistor portion and a surrounding terminal portion. As Fig. 4 shows, the terminal portion is formed in the diffusion layers at the bottoms of 3 trenches, which are then buried by the oxide layer.

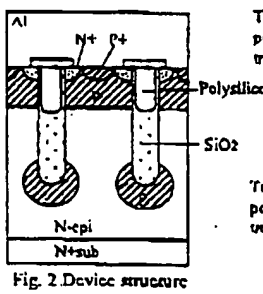


Fig. 2 Device structure

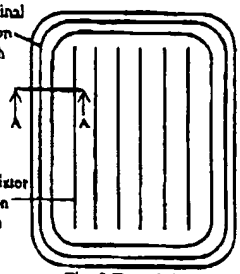


Fig. 3 Trench layout

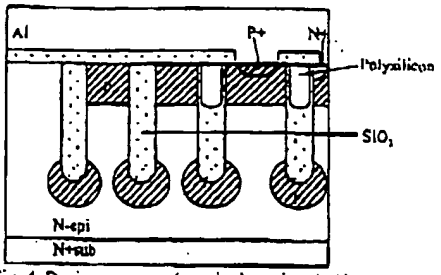


Fig. 4 Device structure (terminal portion A-A)

The structure of a conventional MOSFET is shown in Fig. 5, while Fig. 6 shows the FITMOS structure. The electric field strengths for the devices are shown in Figs. 7 and 8 respectively. In contrast to the conventional MOSFET structure, in which the breakdown voltage is supported at one location, the PN junction as shown in Fig. 7, the FITMOS structure supports the breakdown voltage at two locations, the PN junction between the body and the drift layer and the PN junction between the P layer below the trench and the drift layer, as shown in Fig. 8. This allows for a higher breakdown voltage with the FITMOS structure than with the conventional structure. Where the breakdown voltage is the same, the drift resistance can be lowered by increasing the concentration of impurities in the drift layer.

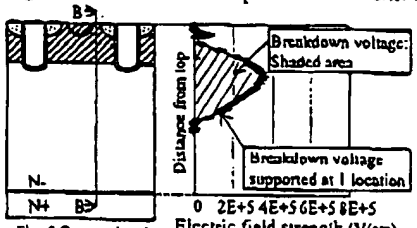


Fig. 5 Conventional MOSFET

Fig. 7 B-B cross section electric field strength

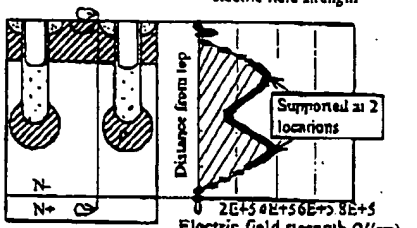


Fig. 6 FITMOS

Fig. 8 C-C cross section electric field strength

Fig. 9 shows the results of a simulation that was done using the simulation model shown in Fig. 10 to show how the on-resistance varies with the trench pitch when the DS breakdown voltage is 70 volts. The trench depth at which the best trade-off between breakdown voltage and on-resistance is achieved was calculated for each trench pitch. It can be seen that the on-resistance is lowest when the trench pitch is from 2 to 2.5μm. The on-resistance of the FITMOS is 40% lower than that of the conventional MOSFET, and the on-resistance value at this point indicates an ultra-low on-resistance characteristic that exceeds the unipolar limit. Also, because the oxide layer in the bottom of the FITMOS trench is thick, its capacitance is low, making it possible to reduce RonQgd. Table 2 shows the results of a simulation of RonQgd. It can be seen that the RonQgd characteristic for the FITMOS is 33% of the conventional MOSFET value.

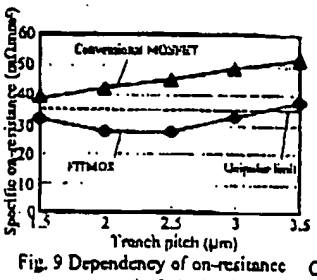
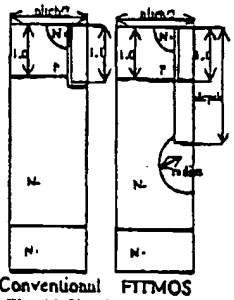


Fig. 9 Dependency of on-resistance on trench pitch (BVdss 70V)



Conventional FITMOS
Fig. 10 Simulation model

Table 2 Figure of Merit (Simulation values)

Item	Conventional(a)	FITMOS(b)	Ratio(b/a)
RonSim	45.2	27.2	0.60
Qgd/Sim	2.4	1.3	0.54
RonQgd	108.5	35.4	0.33

It has been reported that a floating island structure has excellent recovery characteristics (9). It has also been confirmed that the recovery characteristics of the body diode in the FITMOS are excellent. The simulation results are shown in Figs. 11 and 12. The ratio di/dt for the FITMOS is approximately half that for the conventional MOSFET. Fig. 13 shows a simulation result of the hole current flow at point A during reverse recovery. During reverse recovery, holes flow into the floating islands, then are discharged a little at a time. The ratio di/dt is small because the diffusion layer has a buffering effect on the hole flow. The epitaxial thickness of the FITMOS can also be made thinner than that of the conventional MOSFET, so that fewer minority carriers are accumulated in the drift layer and the peak current (I_{Rm}) during reverse recovery can be reduced.

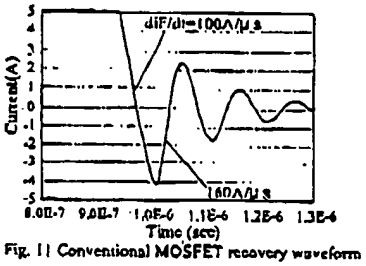


Fig. 11 Conventional MOSFET recovery waveform

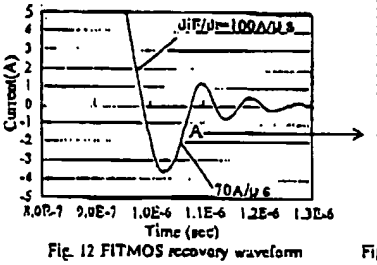


Fig. 12 FITMOS recovery waveform

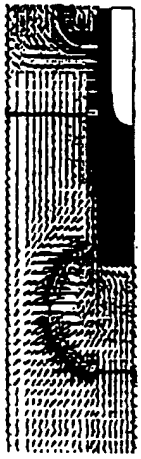


Fig. 13 Hole movement

Fabrication process

Fig. 14 shows the fabrication process: (a) formation of the body diffusion layer and trench etching, (b) formation of the floating islands by means of self-alignment, (c) trench fill with in silicon dioxide and etch back, (d) gate formation, and (e) formation of the source N+, contact P+, and metal. The epitaxial concentration is 2.3E16cm^{-3}, and the epitaxial thickness is 5.5μm. The FITMOS can be fabricated simply by adding steps (b) and (c) above to the conventional MOSFET fabrication process. The breakdown voltage of the terminal portion can be maintained by the same structure that is used in the transistor portion, making it possible to form the transistor portion and the terminal portion at the same time. This means that the number of ion implantation processes can be kept the same as for the conventional MOSFET, and the number of lithographic processes can be reduced. And while it is expected that processes will have to be added to form the diffusion layer in the bottom of the trench and the thick oxide layer in the bottom portion of the trench, the increase in the total number of processes can be kept to around 5%.

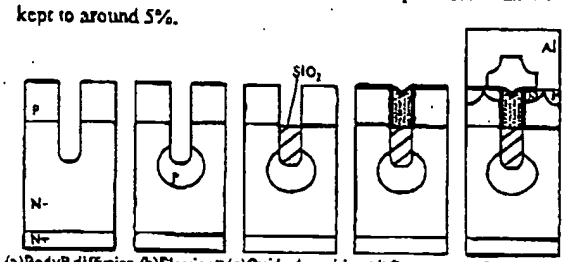


Fig. 14 Schematic process flow

Experimental Results & Discussion

Fig. 15 is a simulation image of the FITMOS process, Fig. 16 is a transmission electron microscope image of the cross section, and Fig. 17 is a scanning capacitance microscope image. The images show that a good shape is obtained.

Fig. 15 Simulation image

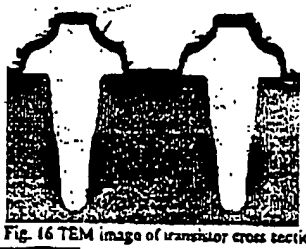


Fig. 16 TEM image of transistor cross section

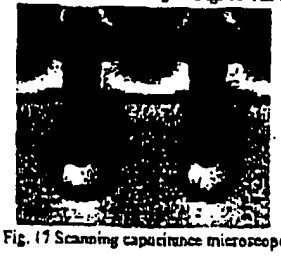


Fig. 17 Scanning capacitance microscope image

Prototypes were made with trench pitches ranging from 2 to 3 μm, and it was confirmed that all operated properly. Figs. 18 and 19 show the DS breakdown voltage characteristics and Id-Vd characteristics for the prototype devices. The DS breakdown voltage is 64 volts (Id: 1mA), the specific on-resistance is 22mΩmm^2 (Vgs: 15V; active surface area: 1.44mm^2; substrate resistance excluded from calculation). Vth is 4 volts (Id: 10mA), and the trench pitch is 2 μm. These results exceed the unipolar limit, and as shown in Fig. 20, constitute the state of the art in this breakdown voltage range.

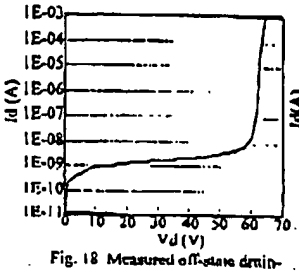


Fig. 18 Measured off-state drain-source current

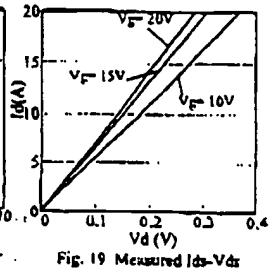


Fig. 19 Measured Ids-Vds characteristics

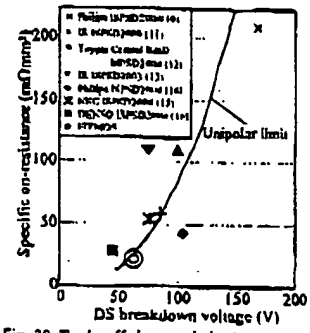


Fig. 20 Trade-off characteristics between specific on-resistance and breakdown voltage

Fig. 21 shows the relationship between the DS breakdown voltage and the distance d between the terminal portion trench and the transistor portion trench, which is illustrated in Fig. 22. It can be seen that d has an optimum value. This indicates that a design is required that maintains a balance of the maximum electric field strength between the body P and the floating islands even in the terminal portion.

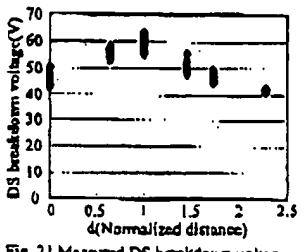


Fig. 21 Measured DS breakdown voltage as a function of the distance d

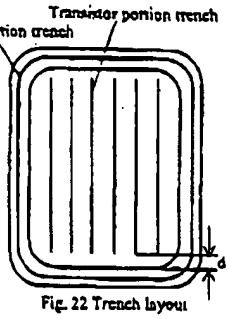


Fig. 22 Trench layout

Fig. 23 shows the on-resistance as a function of temperature. It can be seen that the on-resistance of the FITMOS is much less dependent on temperature than that of the conventional MOSFET. Figs. 24-26 show the capacitances (f=1MHz) of the FITMOS and conventional MOSFET in devices with the same on-resistance. (Conventional MOSFET active area: 23.5mm^2, FITMOS active area: 7.9mm^2) Fig. 27 shows a comparison of the gate charges. Table 3 shows a comparison of the measured values for RonQgd per unit area. The values for the FITMOS are better than those for the conventional MOSFET, and the difference becomes even greater at high temperature, with a FITMOS value for RonQgd at 150°C that is only 16% of the conventional MOSFET value.

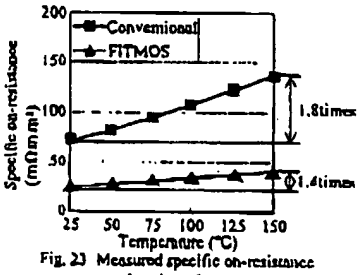


Fig. 23 Measured specific on-resistance as a function of temperature

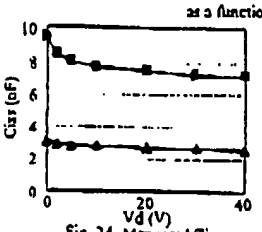


Fig. 24 Measured Ciss

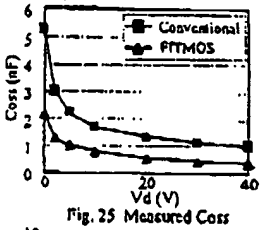


Fig. 25 Measured Coss

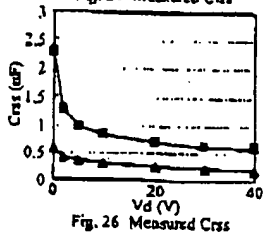


Fig. 26 Measured Crss

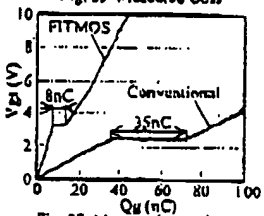


Fig. 27 Measured gate charge (Vd=10V)

Table 3 Figure of Merit (Measured values)

Item	Conventional MOSFET(a)	FITMOS (b)	Ratio (b/a)
RonS(mΩmm^2)	70.0	22.0	0.31
Qgd/S (nC/mm^2)	1.5	1.0	0.67
RonQgd (mΩnC)@25°C	105.0	22.0	0.21
RonQgd (mΩnC)@150°C	189.0	31.0	0.16

Figs. 28 and 29 show the measured recovery waveforms for the conventional MOSFET and the FITMOS respectively. The data confirm that the di/dt ratio for the FITMOS is superior to that for the conventional MOSFET. With the FITMOS, a rate of 98% or better is achieved for non-defective gates in 3-by-4-mm rectangular devices (with active surface areas of 7.9 mm^2) on an 8-inch wafer. This high rate is thought to be a result of the thick oxide layer in the bottom portion of the FITMOS trench, which reduces the surface area of the gate oxide layer, where defects are likely to occur.

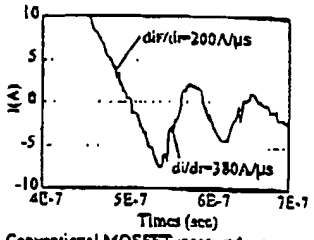


Fig. 28 Conventional MOSFET measured recovery waveform (Active area: 23.5mm^2)

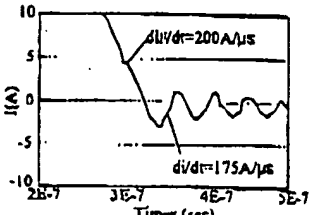


Fig. 29 FITMOS measured recovery waveform (Active area 7.9mm^2)

Conclusions

A new MOSFET structure named FITMOS has been proposed that is characterized by floating islands formed by self-alignment and trench gates with a thick oxide layer on the bottoms. The breakdown voltage is 64 volts, the specific on-resistance is 22mΩmm^2 (Vgs=15V), and the on-resistance characteristics are superior to those of conventional MOSFET. A thick oxide layer in the bottom portion of the trench makes it possible to achieve low gate charge (Qg), so that RonQgd for the FITMOS is only 21% that for a conventional MOSFET. Also, the buffering action of the floating islands at the bottoms of the trenches allows the body diode to exhibit excellent reverse recovery characteristics. Because the terminal portion and the transistor portion of the FITMOS have the same structure, the increase in the number of fabrication processes is less than 5%. Moreover, the rate of non-defective gates in 3-by-4mm rectangular devices on an 8-inch wafer is 98% or higher. The FITMOS is expected to be the premier next generation MOSFET, combining superior characteristics and ease of fabrication.

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